REMARKS

In response to the Office Action mailed on September 6, 2006, Applicant wishes to enter the following remarks for the Examiner's consideration. Applicant has amended claims 1, 9-15, 18-20, 23, 25, 29 and 30 and cancelled claims 4, 5, 7, 16 and 17. Claims 1-3, 6, 8-15 and 18-31 are pending in the application.

Substance of Interview

Applicant has received a copy of the Interview Summary, mailed from the Office on November 21, 2006, pertaining to the telephonic interview conducted between Examiner Denise Tran and Dr. Graham Eatwell on November 2, 2006. In accordance with MPEP Section 713.04, Applicant respectfully disagrees with the examiner's assertion in the Interview Summary form that the Examiner "verified that McDonald et al., e.g., ...teaches 'the first bus protocol is the same as the second bus protocol," claim 1.' Applicant submits for the record that the Examiner made this argument but Applicant's representative, Dr. Eatwell, disagreed with this assertion, for reasons set forth at length below, and thus it is not correct to say that this assertion was "verified."

Objections to the drawings under 37 CFR 1.83(a)

The drawings were objected to under 37 CFR 1.83(a) for not showing every feature of the claim. FIG. 2 shows a bus 108. The specification on page 1, lines 9-15, states "Digital systems often comprise a number of functional blocks connected by one or more bus structures. An example of a functional

block is special purpose accelerator, such as a vector processor or image processor. Functional blocks may be connected using a number of different bus architectures, such as AMBA (Advanced Micro-controller Bus Architecture). AMBA is an open standard, on-chip bus specification that details a strategy for the interconnection and management of functional blocks that make up a System on-Chip (SoC)." Thus, when the bus uses an AMBA it is understood that the functional blocks in FIG. 2 to relate to a SoC, which is an integrated circuit.

However, in order to expedite the issuance of the patent, applicant has amended claims 9-13, 15-24 and 30 to remove references to an integrated circuit. However, it is clear from the above discussion that the digital processing system of the claims could be an integrated circuit, such as a system on a chip (SoC). It is also clear that the digital processing system of the claims could include one or more discrete components.

In the claims 9-13, 15-24, the term 'integrated circuit' has been replaced by the term 'digital processing system'. Support for this amendment is provided by the claims as originally filed. In claim 30, the system bus is defined to be an Advanced High-performance Bus. This amendment is supported by the specification on page 9, lines1-3, for example.

Objections to amendment filed 6/13/06 under 35 USC §132(a)

The amendment filed 6/13/06 has been objected to under 35 USC §132(a). The Applicant respectfully traverses this objection to the amendment in view of the amendments to claims 9-13, 15-24 and 30.

The specification on page 5, lines 12-17 states "The invention may be used with a variety of different bus architectures, but the AMBA will be used as an example. The address translation filter can be inserted between any device that interfaces to an AMBA bus and the AMBA bus. The AMBA bus protocols are robust enough to handle any extra cycles of delay introduced by the filtering device. Such extra cycles appear to the attached device as a slightly slower memory system." Thus it is clear that in one embodiment of the invention the bus in FIG. 2 is an AMBA bus. The Advanced Micro-controller Bus Architecture (AMBA) is an open standard, on-chip bus specification that details a strategy for the interconnection and management of functional blocks that make up a System on-Chip (SoC). This is known to those of ordinary skill in art, and is described in the specification on page 1, lines 9-15, which state "Digital systems often comprise a number of functional blocks connected by one or more bus structures. An example of a functional block is special purpose accelerator, such as a vector processor or image processor. Functional blocks may be connected using a number of different bus architectures, such as AMBA (Advanced Micro-controller Bus Architecture). AMBA is an open standard, on-chip bus specification that details a strategy for the interconnection and management of functional blocks that make up a System on-Chip (SoC)." Thus, when the bus uses an AMBA it is understood that the functional blocks in FIG. 2 to relate to a SoC.

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system on a chip (SoC). It is also clear that the digital processing system of the claims could include one or more discrete components.

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Rejection of claims under 35 USC §112

Claims 9-13, 15-24 and 30 have been rejected under 35 USC §112. Applicant respectfully traverse this rejection of the claims in view of the amendments to claims 9-13, 15-24 and 30, discussed above, which remove all references to an integrated circuit. However, applicant submits that, as discussed above, the digital processing system of the claims could be an integrated circuit, such as a system on a chip (SoC). It is also clear that the digital processing system of the claims could include one or more discrete components.

Claims 29-31 have been rejected under 35 USC §112. Applicant respectfully traverse this rejection of the claims in view of the amendments to claim 29. In claim 29, the term "address translation unit" has been replaced with the term "address translation filter".

Rejection of claims under 35 USC §102

Claims 1-6, 9-19, 21-22 and 24-31 have been rejected under 35 USC §102(a) or 102(e) as being anticipated by McDonald, US Patent Application No. US 2003/0028751. Applicant respectfully traverses this rejection of the claims.

Claim 1, as previously presented, specified that the first bus protocol is the same as the second bus protocol. This element is not disclosed by the McDonald reference. The examiner identifies the bus as connecting between CPU 12 and memory 16 in Figure 1 of the McDonald reference. This bus also connects with the acceleration engine 22 in Figure 1. Figure 3 shows how the bus interface circuit 42 is a shared one of a number of resources 32 shared by accelerators 30A, 30B etc. The bus interface allows the accelerator to connect to the bus. The examiner identifies the interface, inside the accelerator engine, between the shared resources 32 and the accelerators 30 as being equivalent to the second interface. Even if this interface, examples of which are shown in FIG's 4 and 5, were considered to be a bus interface, it would be an interface between the accelerators (30) and a bus and cannot therefore be equivalent the first interface of claim 1, which is an interface between an address translation filter and a bus. McDonald, paragraph 59, states that this interface may be any interface, but again, this an interface between an external device (an accelerator) and a bus, not an interface between an address translation filter and a bus, as called for in claim 1.

The examiner refers to paragraphs 29, 59, 65, 67 and 83. Paragraph 29 only discusses the system bus, shown in figure, external to the accelerator engine 22. Paragraphs 59, 65 and 67 only discuss the interfaces internal to the accelerator engine and do not describe any of the interfaces referenced in paragraph 29. Paragraph 83, in particular, describes how the protocol for the

output from the bus interface circuit 42 may selected from a library of protocols, while the input to bus interface circuit 42, from the accelerators 30A, 30B uses a single common protocol.

In order to expedite the issuance of the patent, Applicant has amended claim 1 to include the limitations of claims 5 and 7. The examiner has indicated that claim 7 is allowable if rewritten in independent form.

Claims 2, 3 and 6 depend from claim 1. Although additional arguments could be made for the patentability of these claims, such arguments are believed to be unnecessary in view of the above discussion.

Claims 4 and 5 have been cancelled. Their limitations have been included in amended claim 1, discussed above.

Claim 9 has been amended to call for the address translation filter to include a translation lookaside buffer, an input for receiving an input system clock signal and an output for transmitting an output system clock signal. Claim 9 has been further amended to specify that output clock signal is paused while the translation lookaside buffer is being refreshed. These elements were included in previously present claim 7, which the examiner has indicated to be allowable.

Claims 10-13 depend from claim 9. Although additional arguments could be made for the patentability of these claims, such arguments are believed unnecessary in view of the above discussion of claim 9.

Claim 14 has been amended to specify that the address translation filter includes a table of physical memory addresses indexed by virtual address, an input for receiving, an input system clock signal and an output for transmitting an output system clock signal, and further amended to specify

that the output clock signal is paused while the table of physical memory addresses is being refreshed. These elements are not disclosed in the McDonald reference and were included in claim 7 that the examiner has indicated to be allowable.

Claim 15 has been amended to specify that translating a virtual memory address specified by the first bus signal to a physical memory address is achieved by selecting a physical memory address from a table of physical memory addresses indexed by virtual addresses and that the table of physical memory addresses is refreshed if the table has no entry for the virtual address. Claim 15 has been further amended to include the elements of transmitting a system clock signal and pausing the system clock signal while the table of physical memory addresses is being refreshed. These elements are not taught by the McDonald reference.

Claims 16-17 have been cancelled and their limitations incorporated into claim 15.

Claims 18 and 19 have been amended to depend from claim 15 discussed above.

Claims and 21-22 depend from claim 15. Although additional arguments could be made for the patentability of each of the claims, such arguments are believed unnecessary in view of the above discussion.

Claim 24 depends from amended claim 9, discussed above. Further, McDonald does not disclose that the shared resources and the accelerators are connected by an AMBA or an AHB.

Claims 25-28 depend from amended claim 14, discussed above.

Claim 29 has been amended to specify that the address translation filter comprises a table of physical addresses indexed by virtual addresses and is operable to pause a system clock supplied to the processing device if the table of physical memory addresses has no entry for a virtual address received from the processing. This element of the claim is not disclosed in the McDonald reference.

Claim 30 has been amended to specify that the system bus comprises an Advanced High-performance Bus. This amendment is supported by the specification on page 9, lines1-3, for example. Claim 30 depends from amended claim 29, discussed above.

Claim 31 depends from amended claim 29 discussed above.

In light of the foregoing amendment and remarks, Applicant respectfully submits that the McDonald reference does not teach, suggest, disclose or otherwise anticipate the recitations of claims 1-3, 5, 6, 9-19, 21-22 and 24-31. Applicant thus respectfully requests that this basis of rejection of the claims be withdrawn and that a Notice of Allowance for these claims be mailed at the Examiner's earliest convenience.

Rejection of claims under 35 USC §103(a)

Claims 8 has been rejected under 35 USC §103(a) as being unpatentable over McDonald et al, US Patent Application No. U.S. 2003/0028751 in view of McGrath, U.S. Patent No. 6,671,791. Applicant respectfully traverses this rejection of the claims in view of the amendments to claim 1, discussed above.

In light of the amendments to base claim 1, Applicant respectfully submits that the McDonald and McGrath references, whether considered alone or in combination fail to teach, disclose, suggest or otherwise render obvious the recitations of claim 8. Applicant thus respectfully requests that this basis of rejection of the claim be withdrawn and that a Notice of Allowance for claim 8 be mailed at the Examiner's earliest convenience.

Allowable claims

Claim 7 has been rewritten in independent form, including all of the limitations of the base claim and the intervening claim, as independent claim 1. Applicant thus respectfully requests that the objection to the claim be withdrawn and that a Notice of Allowance for claim 1 be mailed at the Examiner's earliest convenience.

Claim 20 has been rewritten in independent form, including all of the limitations of the base claim 15 and the intervening claim 17. Applicant thus respectfully requests that the objection to the claim be withdrawn and that a Notice of Allowance for claim 20 be mailed at the Examiner's earliest convenience.

Claim 23 has been rewritten in independent form, including all of the limitations of the base claim 15 and the intervening claim 22. Applicant thus respectfully requests that the objection to the claim be withdrawn and that a Notice of Allowance for claim 23 be mailed at the Examiner's earliest convenience.

In light of the foregoing amendments and explanations, applicant submits that all rejections of claims 1-3, 6, 8-15 and 18-31 have been overcome. Allowance of claims 1-3, 6, 8-15 and 18-31 is therefore respectfully requested at the Examiner's earliest convenience. Although additional arguments could be made for the patentability of each of the claims, such arguments are believed unnecessary in view of the above discussion. The undersigned wishes to make it clear that not making such arguments at this time should not be construed as a concession or admission to any statement in the Office Action.

Please contact the undersigned if you have any questions regarding this application.

Respectfully submitted,

/Renee' Michelle Leveque/

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